

REMARKS

Claims 1-31 are currently pending in the application. By this amendment, claims 1 and 14 are amended and claim 31 is added. The above amendments and added claim does not add new matter to the application and are fully supported by the specification. For example, support for the amendment to claims 1 and 14, and new claim 31 can be found at paragraphs [0018] of the instant published US patent application 2005/02466117. Reconsideration of the rejected claims in view of the above amendments and the following remarks is respectfully requested.

Allowable Claims

Applicants appreciate the indication that claims 10, 11, 23 and 24 contain allowable subject matter. These claims are not being presented in independent form at this time because claims 7 and 20, from which these claims depend, are believed to be allowable. Furthermore, Applicants submit that all of the pending claims are in condition for allowance and that the rejection under § 102 should be withdrawn.

35 U.S.C. § 102(a) Rejection

Claims 1-9, 12-22 and 25-30 were rejected under 35 U.S.C. § 102(a) as being anticipated by the Article entitled "Block-based Static Timing Analysis with Uncertainty" by Anirudh DEVGAN et al. This rejection is respectfully traversed.

In order to establish a *prima facie* case of anticipation under 35 U.S.C. § 102, a single prior art reference must disclose each and every element as set forth in the subject claim. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2

USPQ 2d 1051, 1053 (Fed. Cir. 1987). Applicants respectfully submit that a *prima facie* case of anticipation has not been established as the applied reference fails to teach each and every element of the claims.

More particularly, independent claims 1 and 14 recite, *inter alia*,

wherein the method predicts a delay in circuit paths by considering a portion of the delay that is influenced by a proximity of circuit elements in a path or paths separately from a full delay distribution.

Additionally, independent claims 7 and 20 recites, *inter alia*,

computing a timing slack for the timing test using the at least one location information, wherein the at least one location information comprises a centroid of the one or more inputs to the timing test.

Furthermore, independent claim 27 recites, *inter alia*,

determining a timing slack variation in the early path using location information on one or more elements in the early path, determining a timing slack variation in the late path using location information on one or more elements in the late path, and, computing a new timing slack for the early path and the late path by using the timing slack variation in the early path and the timing slack variation in the late path.

The applied reference does not teach, or even suggest, at least these features.

Applicants acknowledge that DEVGAN discloses a statistical timing analysis wherein "delay and arrival times in the circuit are modeled and as random variables" (see page 608 col. 1, lines 19-21). Applicants also acknowledge that DEVGAN discloses that "critical paths and slack distributions can be computed for a given probability or confidence level" (see page 608, col. 2, lines 9-23). However, it is not apparent that DEVGAN discloses, or even suggests, that the method predicts a delay in circuit paths by considering a portion of the delay that is influenced by a proximity of circuit elements in a path or paths separately from a full delay distribution (claims 1 and

14). Applicants note, in particular, that the Examiner has failed to identify any disclosure in this document indicating that the disclosed analysis even accounts for a proximity of circuit elements in a path or paths, much less, doing so separately from a full delay distribution.

Furthermore, while the Examiner has identified page 610, col. 1, lines 6-17 and pages 610-612, section 3 and Fig. 9 as disclosing that the at least one location information comprises a centroid of the one or more inputs to the timing test (claims 7 and 20), it is apparent that the cited language is silent with regard to utilizing in the analysis a centroid of the one or more inputs to the timing test. Nor has the Examiner explained how such language or the drawing of Fig. 9 can be interpreted to disclose or suggest utilizing a centroid of the one or more inputs to the timing test in the analysis.

Moreover, while the Examiner has alleged that DEVGAN discloses determining a timing slack variation in the early path using location information on one or more elements in the early path, determining a timing slack variation in the late path using location information on one or more elements in the late path, and computing a new timing slack for the early path and the late path by using the timing slack variation in the early path and the timing slack variation in the late path at pages 608-610, the Examiner has failed to identify any specific language in this document in support of such assertions. Applicants note, for example, that while the noted language discusses comparing deterministic arrival times and probabilities thereof (see Fig. 3), there is no apparent disclosure or suggestion indicating that both early and late paths are accounted for, much less, that a timing slack variation thereof is utilized in the analysis.

Nor has the Examiner explained how the noted language can be interpreted to disclose or suggest these features.

Applicants emphasize that whereas DEVGAN uses a statistical probability analysis to determine critical paths and slack distributions, the invention, by way of example, uses actual determined information in the timing test.

Furthermore, dependent claims 2-6, 12, 13, 15-19, 25, 26, 28 and 30 recite additional features which are not disclosed, or even suggested, by DEVGAN and the Examiner has not shown otherwise.

For example, DEVGAN clearly fails to disclose the logic cone of claims 2 and 15, the bounding region recited in claims 3-6, 16-19 and 28, and the abstract location information of claims 12, 13, 25 and 26. In particular, whereas DEVGAN teaches determining the information statistically for paths, it is not correct that DEVGAN teaches gathering one set of information for the entire input cone.

Accordingly, Applicants respectfully submit that the rejection under 35 U.S.C. § 102(a) should be withdrawn.

Comments on Reasons for Allowance

In response to the Statement of Reasons for Allowance set forth in the Office Action, Applicants wish to clarify the record with respect to the basis for the patentability of the indicated claims in the present application. In this regard, while Applicants do not disagree with the Examiner's indication that certain identified features are not disclosed by the references, Applicants submit that the claims in the present application recite a

combination of features, and that the basis for patentability of these claims is based on the totality of the recited features.

New Claims are also Allowable

Applicants submit that the new claim 31 is allowable over the applied art of record. Specifically, claim 31 depends from claim 20 which are believed to be allowable. Additionally, claim 31 recites a combination of features which are clearly not disclosed or suggested by the applied art of record. Accordingly, Applicants respectfully request consideration of these claims and further request that the above-noted claims be indicated as being allowable.

CONCLUSION

In view of the foregoing amendments and remarks, Applicants submit that all of the claims are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue. The Examiner is invited to contact the undersigned at the telephone number listed below, if needed. Applicants hereby make a written conditional petition for extension of time, if required. Please charge any deficiencies in fees and credit any overpayment of fees to Deposit Account No. 09-0456.

Respectfully submitted,
David J. HATHAWAY et al.



Andrew M. Calderon
Registration No. 38,093

March 15, 2006
Greenblum & Bernstein, P.L.C.
1950 Roland Clarke Place
Reston, Virginia 20191
Telephone: 703-716-1191
Facsimile: 703-716-1180